

Patent Assignment Abstract of Title

Total Assignments: 1

Applicati n #: 10025289 **Filing Dt:** 12/19/2001 **Patent #:** NONE **Issue Dt:**
PCT #: NONE **Publication #:** 20030115562 **Pub Dt:** 06/19/200

Inventors: Andrew K. Martin, Narayanan Krishnamurthy

Title: Design verification system for avoiding false failures and method therefor

Assignment: 1

Reel/Frame: 012410/0262 **Received:** 01/04/2002 **Recorded:** 12/19/2001 **Mailed:** 02/22/2002 **Pages:**

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: MARTIN, ANDREW K.

Exec Dt: 12/19/2001

KRISHNAMURTHY, NARAYANAN

Exec Dt: 12/19/2001

Assignee: MOTOROLA, INC.

LAW DEPARTMENT

1303 EAST ALGONGUIN ROAD

SCHAUMBURG, ILLINOIS 60196

Correspondent: MOTOROLA, INC.

JOANNE G. CHIU

7700 W. PARMER LANE

MD: TX32/PL02

AUSTIN, TX 78729

Search Results as of: 8/11/2003 10:15:55 A.M.

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
4	BRS	L4	1	functional same equivalence same verification same constraints	USPAT; US-PGPUB	2003/08/11 10:08			0
5	BRS	L5	57	functional same equivalence same verification	USPAT; US-PGPUB	2003/08/11 10:09			0
6	BRS	L6	4	equivalence same verification same circuit and	USPAT; US-PGPUB	2003/08/11 11:24			0